

FORM PTO-1449/A and B (Modified)		APPLICATION NO.: 09/477,790	ATTY. DOCKET NO.: S1022/8363
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> JUN 22 2001 PATENT & TRADEMARK OFFICE		FILING DATE: December 31, 1999	
		APPLICANT: Geoff Barrett	
		GROUP ART UNIT: 2819	EXAMINER:
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### U.S. PATENT DOCUMENTS

Examiner's Initials#	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication or of Issue of Cited Document MM-DD-YY
		Number	Kind Code		
H.D		4,376,299		Rivest	03/08/83
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H.D		5,831,853		Bobrow et al.	11/03/98

### FOREIGN PATENT DOCUMENTS

Examiner's Initials#	Cite No.	Foreign Patent Document			Name of Patentee or Applicant of Cited Document (not necessary)	Date of Publication of Cited Document MM-DD-YY	Translation (Y/N)	
		Office/Country	Number	Kind Code				
H.D		EP	0 653 716	A1		05/17/95		

### OTHER ART — NON PATENT LITERATURE DOCUMENTS


Examiner's Initials#	Cite No	Include name of the author (in CAPITAL LETTERS) title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, relevant page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)
H.D		Standard Search Report issued by the European Patent Office, dated November 11, 1997	
H.D		Hu et al., <i>New Techniques For Efficient Verification With Implicitly Conjoined BDDs</i> , Proceedings of the IEEE Design Automation Conference, San Diego, California, June 6-10, 1994, pp. 276-282	

EXAMINER <i>Herzog de Day</i>	DATE CONSIDERED <i>12/30/02</i>
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H.D		Peng et al., <i>Reachability and Reverse Reachability Analysis of CFSMs</i> , Computer Communications, Vol. 19, No. 8, July 1996, pp. 668-674		
H.D		Takahara et al., <i>A Higher Level Hardware Design Verification</i> , Proceedings of the 1988 IEEE International Conference on Computer Design: VLSI in Computers and Processors, Rye, New York, October 3-5, 1988, pp. 596-599		
H.D		Jain et al., <i>Hierarchical Constraint Solving in the Parametric Form with Applications to Efficient Symbolic Simulation Based Verification</i> , Proceedings of the 1993 IEEE International Conference on Computer Design: VLSI in Computers and Processors, Cambridge, Massachusetts, Oct. 3-6, 1993, pp. 304-307		
H.D		Aziz et al., <i>Minimizing Interacting Finite State Machines: A Compositional Approach to Language Containment</i> , Oct. 10-12, 1994, pp. 255-261, IEEE XP000488900		
H.D		Coudert et al., <i>Verification of Sequential Machines Using Boolean Functional Vectors</i> , Dec. 13, 1989, Int. Workshop on Applied Formal Methods for Correct VLSI Design		
H.D	C8	Vai et al., <i>Qualitatively Modeling Heterojunction Bipolar Transistors For Optimization: A Neural Network Approach</i> , IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, 1993, pp. 219-227		
H.D	C9	Wu et al., <i>A Massively Parallel Reverse Modeling Approach For Semiconductor Devices And Circuits</i> , IEEE/Cornell Conf. On Advanced Concepts in High Speed Semiconductor Devices and Circuits, 1997, pp. 201-209		
H.D		Vai et al., <i>Reverse Modeling Of Microwave Circuits With Bidirectional Neural Network Models</i> , IEEE Transactions on Microwave Theory and Techniques, Vol. 46, No. 10, October 1998, pp. 1492-1494		

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